ISSN 2229-5518

Design Consideration of Dual Threshold Logic for High Performance and Ultralow Power Carry Look-Ahead Adder

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Abstract— This paper presents the design of high performance and ultralow power 8-bit carry-look-ahead adder circuits using two-phase modified dual-threshold voltage (dual-V_T) domino logic method with the feed through logic concept. The proposed concepts are provides lower delay and dynamic power consumption; due to these two advantages it perform better in high fan-out and high switching frequencies. The FTL logic functions can be cascaded in a domino-logic without a need for the intervening inverters. The PMOS high threshold V_T keeper increases the circuit speed and reduces the average power consumption. In addition NMOS switch added for avoiding charge sharing problem in pre-charging mode. The additions of two 8-bit binary operands are executed in two cycles. It found that, the circuit is suitable for long adders; the dynamic power consumption is also drastically reduced by more than 50% by the measurement results. This proposed CLA method reducing power (50%) and propagation time delay (around 20%).

Index Terms— Carry look-ahead adder (CLA), CMOS; Domino logic, Dual-threshold voltage (dual-V_T), FTL logic, Pipeline, Programmable logic array (PLA).

1 Introduction

As the demand for higher performance CMOS VLSI processors with increased complicating grows, we need to improve the performance, area efficiency, and functionality of arithmetic circuits. High speed adders are key elements in digital circuits, like multipliers, microprocessor unit (MPU), application specific integrated circuit (ASIC) designs, and digital signal processing (DSP) chips. Many efforts have been focused on the improvement of adder designs. Since, the use of carry look-ahead (CLA) principle for high speed arithmetic units are remains dominant. One of the challenges in VLSI processor design today is to structure multilevel CLA circuits, specifially for 8-bit integrated circuits without limiting the functional flexibility.

A low power high performance circuit technique was proposed in [1] for reducing power dissipation and diminishing propagation delay of domio logic circuits. The low power FTL dynamic logic is achieved by feedthrough dynamic CMOS logic structure [2]. Wang, Tsai [3] employed 8-bit CLA using dual-V_T domino logic blocks which are arranged in a PLA- like manner and synchronously triggered. It is implemented on silicon to verify the power reduction as well as the preservation of high speed. Huang, li lee [4] proposed an 8-bit pipelined CLA using the dual-V_T domino logic blocks for low power logics. Dual-V_T domino logic circuits proposed for reucing subthreshold leakage current in domino logic circuits is proposed in [5].

Domino logic is widely used in high performance integrated circuits. It reduces the device count, silicon area and improves the performance of integrated circuits when compared to the standard fully complementary static CMOS logic circuits. However, the major drawback with the domino dynamic logic circuit is its excessive power decipation due to the switching activityand the clock load. To deal with the excessive power dissipation of the dynamic logic, the current design methodologies are employed with power for performance in the delay critical sections of the circuit. This is achieved through a mix of dynamic and static circuit styles, use of dual supply voltages and dual-V_T transistors. Domino and dynamic logic's are mainly affected by charge sharing and race problems. The proposed circuits are giving solution for these problems and minimizing power wastages. In this paper we propose a design consideration of dual threshold logic for ultralow power high performance CLA logic structure.

2 Modified Dual-V_T Domino Logic Circuits

Dual-V_T Domino Logic Circuits proposed for reducing sub threshold leakage current and power in domino logic circuits [5]. Low power FTL logic is presented in [1]. By utilizing this logic's, we proposed our new low power dual high-V_T domino logic circuits as shown in Fig 1(a) and (b). The domino logic operation is divided into two phases: precharge phase and evaluation phase. In circuit having NMOS logic network (NMOS block), an NMOS transistor (N11) for resetting the output node to low logic level, together with a pull up PMOS load transistor P11. N11 and P11 are controlled by the clock pulses (Clock). The NMOS keeper is used to operate the circuit with minimum delay.

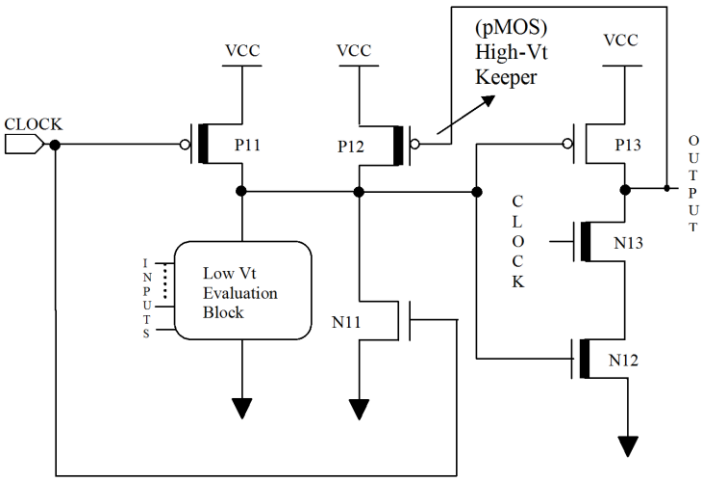


Fig 1(a): Proposed dual-V_T domino logic I

2.1 Propsed Logic I

1) During the precharge phase when clock=0, P11 is on and N11 is off. Then, node (A) is pre-charges towards VDD. The output is kept into previous stage by the clock controlled N13.

2) During the evaluation phase when clock=1, P11 is off and N11 is on. If the low-Vt evaluation block is evaluated to be passing the charge at node A should be ground through the low-Vt evaluation block and N11. The output then is logic high. If the low-V_T evaluation block is evaluated to be stop there will be no discharging path for node A. A keeper PMOS, P12, is added to keep node A at VDD. Then, the output goes to logic low.

A clock-controlled NMOS transistor, N13 in Fig.1 (a), is inserted in the discharging path of the output inverter. The operation of the modified dual-V_T domino logic circuit is similar to that of the typical dual-V_T domino logic circuit apart from the pre-charge phase. During the pre-charge phase, clock= 0, P11 is on, N11 and N13 are both off. Thus, P12 is switched off. The output has neither charging path nor discharging path such that the state will be kept as the previous state. This also results in that the circuit to consume less power.

2.2 Propsed Logic II

Fig 1(b): Proposed dual-V_T domino logic II

The proposed low power circuit is shown in Fig 1(b). It consists of an NMOS logic network (NMOS block), an NMOS transistor (N21) for resetting the output node to low logic level, together with a pull up PMOS load transistor (P21). N22 and P21 are controlled by the clock signal. N21 is used to control the charge sharing problem; this high Vt NMOS transistor blocks charge sharing while in pre-charging phase.

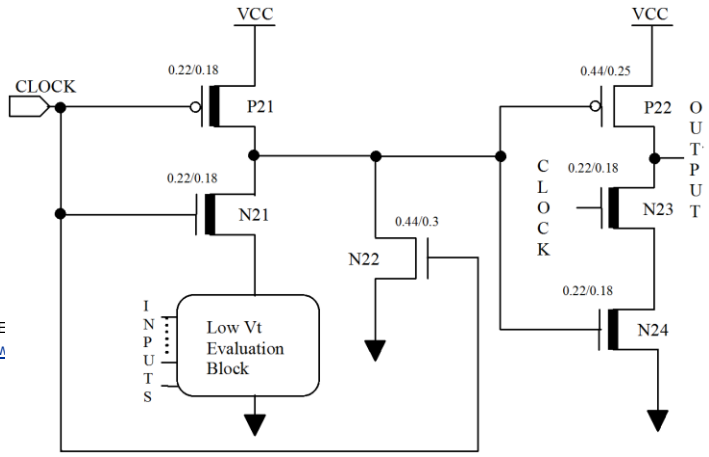
High V_T NMOS switch is driven by clock signal. The proposed dynamic logic family is allows to perform the partial evaluation of a computational block before its input signals are valid, and then quickly performs a final evaluation as soon as the inputs arrive. The proposed dynamic logic family is well suited for arithmetic circuits where the critical path is made up of a large cascade of inverting gates.

Consider a long chain of inverters as shown in [1]. When the clock signal falls, the outputs of the cascaded gates begin to raise the gate threshold voltage to V_{TH} [1]. At this voltage all the gates in the circuit are in a high gain point. This feature distinguishes the proposed logic family from the other dynamic logic families. At V_{TH} point any small variation in the input nodes would cause a fast variation of the voltage at the output node. In all other logic families for the output node to begin transition, the inputs need to cross the threshold voltage.

Furthermore, when the valid inputs to a gate are asserted, the gate outputs will only need to make a partial transition from V_{TH} to V_{OH} or V_{OL} through the validation of evaluation block. The higher performance of the proposed logic circuit is achieved by reducing the propagation delay of both low-to-high and high-to-low transition. However, maintaining the V_{TH} stability for long cascaded circuit structures is a main challenge in this proposed logic, which is the key factor in the fast logic evaluation and high performance of the proposed circuits. In the integrated circuits, V_{TH} stability of cascaded circuit can be achieved by manufacturing technology.

2.3 PLA Styled 8-bit CLA design

If the propagate signals (Pi) and the generate signals (Gi) of a CLA are produced by combinatorial logic function blocks before they are fed into the function blocks for S_i's and C_i's, then the Boolean equations of S_i's and C_i's imply that a two-level AND-OR logic function block is a possible solution to achieve high speed operations. Thus, the PLA styled design is suitable for such a function block. A conceptual PLA styled design for CLA is shown in Fig.3. A typical PLA consists of an AND array and an OR array. It is well known that the series NMOS in the evaluation block of NAND or AND gates will produce long discharging delays which subsequently slow



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down the entire circuit.

We can take advantage of the non-inverting feature of the domino logic to utilize an OR-NOT configuration instead of the typical AND-OR style, where the two OR planes are made of the modified dual-V_T domino logic circuits as shown in Fig 1(b). Meanwhile, it can also minimize the series transistor count in the low-V_T evaluation block. The OR array is made up of modified dual-V_T domino logic with a predefined low-V_T evaluation block.

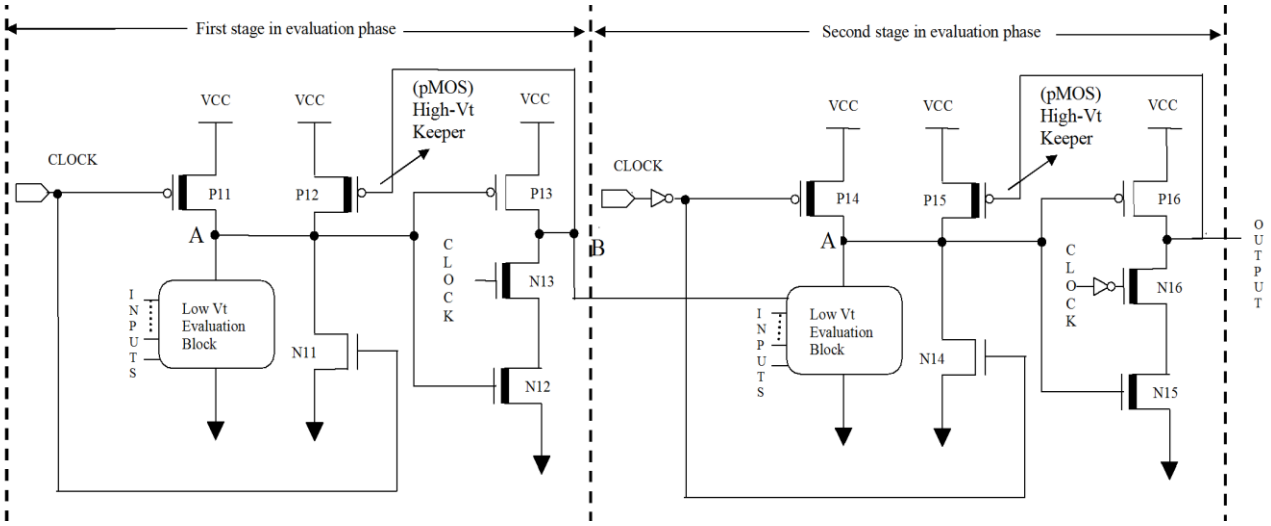


Fig 2: Two stages of proposed dual-VI domino logic I

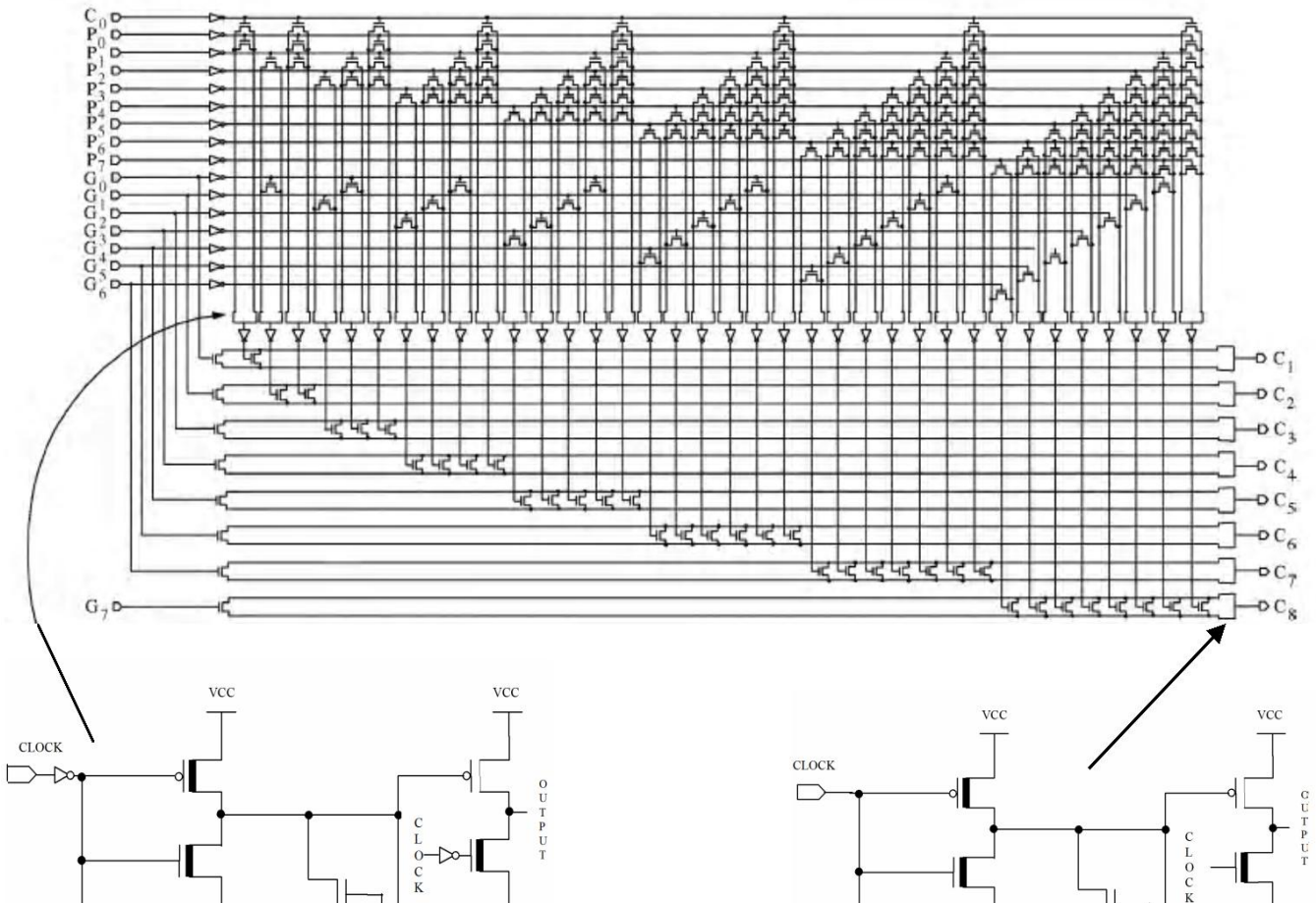
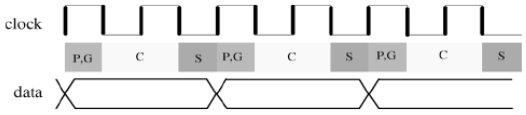


Fig 3: PLA – Styled carry lookahead adder

The inputs to the first OR array is the inverted P_i's and G_i's signals which are also produced by other modified dual-V_T domino logic units as shown in Fig 4. Notably, we define the propagate signals in a different way from the traditional Pi = $A_i + B_i$, because the $P_i = A_i B_i$ can be reused to generate the sum term, i.e., S_i.



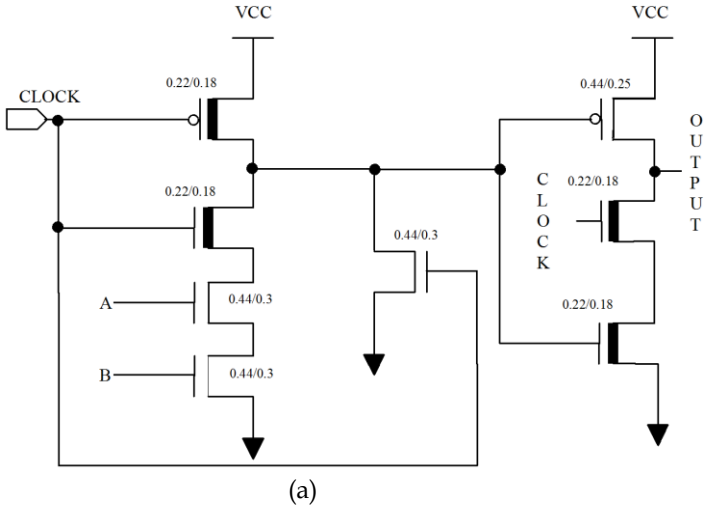
g 4: (a) G block (b) P block

i

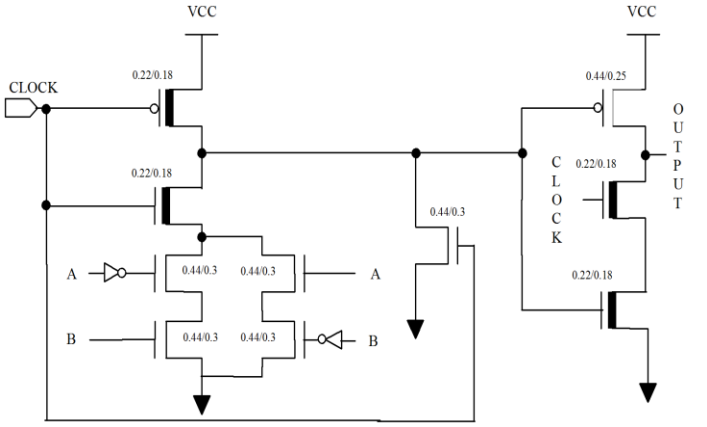
3 Cycle Based Operation and Area Analysis

3.1 Cycle Based Operation

The critical path of an adder resides on the generation of carry signals, i.e., C_8 in the 8-bit adder. After the binary operands are ready, the generation of P_i's and G_i's by using the modified dual-V_T domino logic takes the high half of a full cycle. That is, the results of G and P-blocks will be ready when the clock is low.



(a)



The inverted Pi's and Gi's will then be fed into the first OR plane of the modified dual-VT domino-based PLA. The inverted outputs of the first OR plane will be presented to the second OR at the high half of the second cycle. The final Ci's results then are ready in the low half of the second cycle. Right after the generation of every Ci's, they are inverted and fed into the Si's function blocks. Another half cycle then is required to produce all of the Si's. The final result will be latched after two cycles as shown in Fig 5.

Fig 5: Operation timing diagram of the PLA-styled CLA

3.2 Area

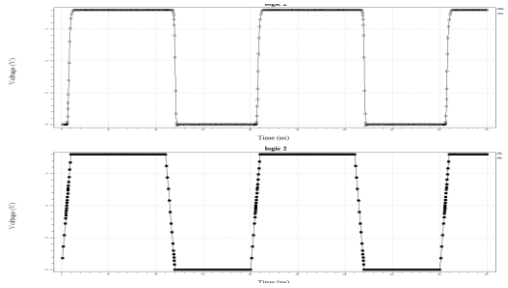
The transistor count of the PLA-styled implementation for CLA using All-N-Transistor (ANT) logic, an analytic form has been derived in [10]. By the similar derivation method, the number of the total transistors required to implement the proposed n-bit CLA with PLA-styled design using the modified dual- V_T domino logic is as follows,

$$T_{Total} = \left(\frac{1}{6}\right)(n+1)(n+2)(n+3) + \left(\frac{9}{2}\right)n(n+1) + 48n + 9 \qquad (1)$$

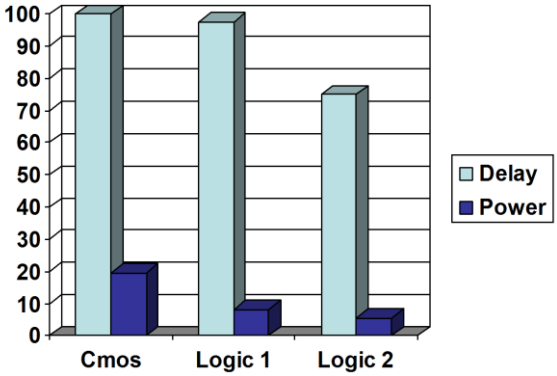
For instance, for an 8-bit adder using our proposed design, the overall transistor count is 882.

3 SPICE Simulation Results

The input and output waveform and comparison chart shown in fig.6. The proposed high performance and low power 8-bit carry-lookahead adder technique increases the circuits speed and reduces the average power consumption. To verify this assertion, simulations were conducted for both circuits of Fig 1(a) and (b). A TSMC 0.18 mm CMOS technology was employed in tanner EDA tool.



(a)



(b)

Fig.6 (a) Output waveform of logic circuit (o/p & i/p),
(b) Comparison chart

The power and delay values are verified using following formulas.Transient power consumption can be calculated using the equation:

$$Power\ (P_T) = C_{PD} \times V_{CC} \times f_I \times N_{SW} \quad (2)$$

Where:

P_T → Transient power consumption,
V_{CC} → Supply voltage,
f_I → Input signal frequency,
N_{SW} → Number of bits switching,
C_{PD} → Dynamic power-dissipation capacitance.

In the case of single-bit switching, NSW in equation is considered as 1. Figure of merit of the circuit is measured by,

$$Figure\ of\ merit = Delay \times Power \times Area \quad (3)$$

The average propagation delay (TPD) is defined as,

$$T_{PD} = \left(\frac{T_{PDR} + T_{PDF}}{2} \right) \quad (4)$$

Where,

T_{PDR}: Rising propagation delay
From input to rising output crossing VDD/2.
T_{PDF}: Falling propagation delay
From input to falling output crossing VDD/2.

4 Conclusion

In this paper, we have presented an efficient method to minimize power and increase the speed in CLA using dual- Vt and FTL CMOS logic technique. Charge sharing problems associated with dynamic and domino families are also removed in the proposed structures. By avoiding these power wastages and dual Vt domino logic technique reduced the total power consumption of circuit. Experiments have shown that high speed and low power obtained by the proposed model match with SPICE simulation results very well. By the experimental verification, the proposed CLA method reduced power more than (60%) and propagation time delay (around 20%).

Acknowledgment

The successful completion of any task would be incomplete without the mention of the people who made it possible through their constant guidance and and encouragement crowns all the efforts with success. Most of all, we are very much thankful to **Our Parents** and **Family members** whose consistent encouragement, moral support and blessings made to finish this thesis work on time. With great pleasure and privilege I express my sincere thanks to **Mr.R.Sakthivel,** Asst. Professor (SG), School of Electrical Sciences, VIT Vellore, for his Omni directional guidance throughout the project. We would also like to express our gratitude towards our fellow staff members and students who helped us in every possible way to make this project a success. We express our heartfelt thanks to the V**IT University** and the Management of the Institution for their potential support and provide a good environment and infrastructure to successful completion of the project.

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